The opinion in support of the decision being entered today
is *not* binding precedent of the Board

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte PAUL E. MCKENNEY, BENEDICT JACKSON,
RAMAKRISHNAN RAJAMONY and RONALD L. ROCKHOLD

Appeal 2007-1600
Application 09/753,062[1]
Technology Center 2100

Decided: September 27, 2007

Before: LEE E. BARRETT, HOWARD B. BLANKENSHIP,
and MARC S. HOFF, *Administrative Patent Judges*.

HOFF, *Administrative Patent Judge.*

DECISION ON APPEAL

STATEMENT OF CASE

Appellants appeal under 35 U.S.C. § 134 from a Final Rejection of claims 1-31. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm-in-part.

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[1] Application filed December 28, 2000. The real party in interest is International Business Machines Corporation.

Appellants' invention relates to a method and system for efficiently handling high contention locking in a multiprocessor system. "Locking" refers to the designation of one of the processors in a multiprocessor system as the processor entitled to access shared memory resources at any particular instant in time. In Appellants' invention, the processors are organized in a hierarchical manner, wherein granting of an interruptible lock to a processor is based upon the hierarchy (Specification 1).

Claim 1 is exemplary:

1. A method for efficiently handling high contention locking in a multiprocessor computer system, comprising:

organizing at least some of the processors into a hierarchy;

providing a lock selected from the group consisting of: an interruptible lock, and a lock which waits using only local memory; and

processing the lock responsive to the hierarchy.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Kermani	US 6,163,831	Dec. 19, 2000

Claims 1-31 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Kermani.

Appellants contend that the Examiner erred because the processors or agents of Kermani are not organized in a hierarchy as claimed by

Appellants, and because Kermani does not teach (a) a data structure or bit mask, (b) a release flag, and (c) a handoff flag. The Examiner contends that the priority assigned to the agents/processors of Kermani may fairly be characterized as a hierarchy, and that Kermani teaches all the elements of the claimed invention.

Rather than repeat the arguments of Appellants or the Examiner, we make reference to the Briefs and the Answer for their respective details. Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants could have made but chose not to make in the Briefs have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2004).[2]

ISSUE

The principal issue in the appeal before us is whether a "hierarchy" encompasses a set of items having a priority established among them.

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[2] Appellants have not presented any substantive arguments directed separately to the patentability of the dependent claims or related claims in each group, except as will be noted in this opinion. In the absence of a separate argument with respect to those claims, they stand or fall with the representative independent claim. *See In re Young,* 927 F.2d 588, 590, 18 USPQ2d 1089, 1091 (Fed. Cir. 1991). *See also* 37 C.F.R. § 41.37(c)(1)(vii).

FINDINGS OF FACT

The following Findings of Fact (FF) are shown by a preponderance of the evidence.

The Invention

1. Appellants invented a method and system for efficiently handling high contention locking in a multiprocessor system (Specification 1).

2. The processors of the multiprocessor system are organized in a hierarchical manner, wherein granting of an interruptible lock to a processor is based upon the hierarchy (Specification 1).

3. Appellants' Specification contains no specific definition of the term "hierarchy."

Kermani

4. Kermani teaches an arbiter for a shared synchronous memory, comprising an arbitration module to select one of a plurality of requesting agents (i.e., processors) for access to the shared synchronous memory (col. 2, ll. 46-49).

5. Kermani teaches a plurality of agents, each of which sends a memory access request to arbiter 102a, which includes a priority encoder 190 (Fig. 2; col. 4, ll. 11-57).

6. A memory access request by an agent (processor) is a digital signal that indicates that a particular agent desires access to the shared synchronous memory (col. 4, ll. 33-45).

7. If more than one memory access request signal is received by the arbiter during any one clock cycle, a winning agent is selected based on a

plurality level assigned to each of the requesting agents. Preferably, a unique priority level is established for each of the plurality of agents either before operation of the system or on-the-fly as the system is operated. Alternatively, a priority level can be assigned to each of the agents using a hardwired encoder in the arbiter (col. 4, ll. 46-57).

8. When the "super agent" (having highest priority) is not accessing the shared synchronous memory, an open window is generated allowing the other non-super agents free access to the shared synchronous memory in accordance with the time slots determined by a free-running clock (col. 6, ll. 23-27).

9. The super agent is provided transparent access to the shared synchronous memory whenever desired, without arbitration or negotiation (col. 6, ll. 8-11).

PRINCIPLES OF LAW

Anticipation is established when a single prior art reference discloses expressly or under the principles of inherency each and every limitation of the claimed invention. *Atlas Powder Co. v. IRECO Inc.*, 190 F.3d 1342, 1347, 51 USPQ2d 1943, 1946 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79, 31 USPQ2d 1671, 1673 (Fed. Cir. 1994).

ANALYSIS

Appellants argue that Kermani does not anticipate the claims because "the processors or agents[3] of Kermani are not organized in a hierarchy as claimed by Applicants" (Br. 4). Appellants acknowledge that Kermani

[3] Kermani uses the terms "agent" and "processor" interchangeably to refer to the same elements.

teaches that a winning agent is "selected on a priority level assigned to each of the requesting agents," but insist that Kermani does not meet the limitation of "organizing at least some of the processors into a hierarchy" because "[a] priority may be assigned within a hierarchical structure, however, the use of a hierarchical structure does not necessitate the assignment of a priority to any element within the hierarchical structure" (Br. 4).

We disagree with Appellants. The question is not whether the use of a hierarchical structure necessitates the assignment of priority, but rather whether Kermani's disclosed organization of processors as prioritized, one above another, meets the claimed "hierarchy." The answer to the question turns on the meaning of "hierarchy."

We note at the outset that the term is not defined in the Specification. In response to the Office Action mailed April 21, 2004, Appellants submitted a definition of "hierarchy," from a text on Java programming, as "an organizational technique in which items are layered or grouped to reduce complexity."[4] Appellants' Brief includes graphical exhibits of the priority ranking of Kermani and the hierarchy ranking of the instant invention (Br. 5, Figs. 1 and 2). Kermani teaches a straight-line arrangement of, e.g., seven elements, #1 being above #2, which is above #3, etc. down to #7 (see FF 7), whereas the depiction of the inventive hierarchy is in the form of a binary tree, with one element at the topmost layer, two elements at the next layer, and so on, with two elements branching from each one above. Appellants

[4] John Lewis and William Loftus, Java Software Solutions: Foundations of Program Design 669 (3rd ed. 2003); definition submitted with response to non-final Office action, filed July 22, 2004.

argue that "[t]here is no provision in the system of Kermani for grouping agents at an assigned priority level since each agent is assigned a unique priority," and that "Kermani does not provide for a structure in which items are layered or grouped" (Br. 6).

While we agree that Kermani does not teach grouping agents at an assigned priority level, that fact is irrelevant to patentability because no claim requires such grouping, and because Appellants' proffered definition of "hierarchy" only requires layering *or* grouping, in the alternative. We find that Kermani's priority scheme constitutes the layering of agents, one above another, one agent per layer, and as such Kermani's prioritization of agents is equivalent to organizing processors into a hierarchy. We therefore find that, even under Appellants' latest suggested definition of "hierarchy," Kermani teaches the limitations of claim 1.

We further note that Appellants submitted a different definition of "hierarchy," in response to a previous Office Action, as "any arrangement of principles, things etc. in an ascending or descending order."[5] It is immediately apparent from Figure 2 of Appellants' Brief (Br. 5) that Kermani's priority scheme meets this more common definition of the word "hierarchy." As a result, under either definition of "hierarchy" advocated by Appellants, we find that Kermani teaches the limitations of claim 1.

We therefore affirm the Examiner's rejection of claim 1 under 35 U.S.C. § 102. We further affirm the rejections of claims 2-8, 13-19, 20, and 22-28, grouped with claim 1 and not argued separately by Appellants.

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[5] WEBSTER'S DICTIONARY 456 (encyclopedic ed. 1989), submitted with Appellants' response to non-final Office Action, filed Feb. 5, 2004.

With respect to claims 9 and 10, Appellants argue that Kermani lacks any teaching of a "data structure" or "bit mask," let alone such an item indicating which processor is waiting for the lock. We agree that the specific terms are not present in Kermani. Fig. 2 of Kermani, however, illustrates a plurality of agents (numbered 1-*n*), each of which sends a memory access request to arbiter 102a, which includes a priority encoder 190 (FF 5). A memory access request by an agent is a digital signal that indicates that said agent desires access to the shared synchronous memory (FF 6). As is well known in the art, a priority encoder operates by receiving a plurality of inputs (bits), and selecting the input having the highest priority. We find that the set of memory access request signals, taken together, may fairly be characterized as a "data structure" having a "bit mask" indicating which processors (agents) are waiting for the lock (i.e., waiting to access shared synchronous memory). We therefore affirm the Examiner's rejection of claim 9, as well as the Examiner's rejection of claim 10, not separately argued by Appellants.

With respect to claims 11, 20, and 30, Appellants argue that there is no express or inherent teaching in Kermani of the use of a release flag to prevent races between processors between acquisition and release of a lock (Br. 9). We agree with Appellants. While the section of Kermani cited by the Examiner (see FF 8) does discuss an "open window" generated when super agent A is not accessing the shared synchronous memory, there is no teaching of a "release flag" or any other mechanism in Kermani to prevent

races between processors. We therefore reverse the rejection of claims 11, 20 and 30 under 35 U.S.C. § 102.[6]

With respect to claims 12, 21 and 31, Appellants argue that there is no teaching of maintaining a handoff flag for a group of processors to grant the lock to a processor requesting an unconditional lock from a processor requesting a conditional lock (Br. 10). We agree with Appellants. Kermani teaches that super agent A may have access to the shared synchronous memory whenever desired (FF 9), but does not teach or suggest unconditional or conditional locks, or the handoff of locks from one processor to another. Accordingly, we reverse the rejection of claims 12, 21 and 31 under 35 U.S.C. § 102.[7]

CONCLUSION OF LAW

We conclude that Appellants have not shown the Examiner erred in rejecting claims 1-10, 13-19 and 22-29. Claims 1-10, 13-19, and 22-29 are not patentable. We conclude that Appellants have shown the Examiner erred in rejecting claims 11, 12, 20, 21, 30, and 31. On the record before us, claims 11, 12, 20, 21, 30, and 31 have not been shown to be unpatentable.

DECISION

The Examiner's rejection of claims 1-10, 13-19, and 22-29 is affirmed. The Examiner's rejection of claims 11, 12, 20, 21, 30, and 31 is reversed.

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[6] We note the absence of a rejection of claims 11, 20, and 30 under 35 U.S.C. § 103.

[7] We note the absence of a rejection of claims 12, 21, and 31 under 35 U.S.C. § 103.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. §1.136(a). See 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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